Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claims 1 – 75 (Cancelled)

76. (New) A method for providing ordered capture clocks to detect or locate faults within N clock domains and faults crossing any two clock domains in an integrated circuit or circuit assembly in self-test mode, where N > 1, each clock domain having one capture clock and a plurality of scan cells, each capture clock comprising a plurality of shift clock pulses and capture clock pulses; said method comprising the steps of:

(a) generating and shifting-in N pseudorandom stimuli to all said scan cells within said N clock domains in said integrated circuit or circuit assembly during a shift-in operation;

(b) applying an ordered sequence of capture clocks to all said scan cells within said N clock domains, the ordered sequence of capture clocks comprising at least two said capture clock pulses from two or more selected capture clocks placed in a sequential order, wherein each said selected capture clock must contain at least one said capture clock pulse and does not contain any said shift clock pulse, during a capture operation; and

(c) compacting N output responses of all said scan cells to signatures during a compact operation.

77. (New) The method of claim 76, wherein each said capture clock is programmable to contain one or more clock pulses for performing said shift-in/compact and capture operations on all said scan cells within one said clock domain; wherein said clock domain is solely controlled by said capture clock; and said capture clock can be either generated internally or controlled externally, and can operate either at its rated clock speed (at-speed) or at a selected clock speed.

78. (New) The method of claim 76, further comprising providing N scan enable (SE) signals each within one said clock domain; wherein said SE signals are used to switch operations from shift-in/compact to capture, and vice versa; and further said SE signals can be generated internally or controlled externally, and are operated either at the rated clock speeds or at selected clock speeds.

79. (New) The method of claim 78, wherein said providing N scan enable (SE) signals further comprises using one global scan enable (GSE) signal to drive said N scan enable (SE) signals so that all said GSE and said SE signals can be operated at a selected reduced clock speed.

80. (New) The method of claim 76, wherein said generating and shifting-in N pseudorandom stimuli further comprises operating all said N capture clocks at selected clock speeds or at the same clock speed; wherein all said N capture clocks are selectively skewed so that at any given time only scan cells within one or more said clock domains are changing states to reduce power consumption.

81. (New) The method of claim 76, further comprising the step of comparing said signatures with their expected signatures for error indication, after a predetermined limiting criterion is reached; wherein said step of comparing said signatures with their expected signatures further comprises comparing said signatures inside said integrated circuit or circuit assembly or shifting-out said signatures for comparison in an ATE (automatic test equipment).

82. (New) The method of claim 76, wherein said generating and shifting-in N pseudorandom stimuli further comprises using a plurality of pseudorandom pattern generators (PRPGs) to generate said N pseudorandom stimuli.

83. (New) The method of claim 82, wherein said pseudorandom pattern generator (PRPG) further comprises using a phase shifter connected to said PRPG outputs to generate one or more said pseudorandom stimuli.

84. (New) The method of claim 83, wherein said phase shifter is a linear logic network comprising one or more Exclusive-OR (XOR) or Exclusive-NOR (XNOR) gates.

85. (New) The method of claim 76, wherein said applying an ordered sequence of capture clocks further comprises applying two or more said capture clocks concurrently on clock domains which do not interact with each other or have any logic block crossing each other for detecting or locating said faults in said clock domains controlled by said capture clocks.

86. (New) The method of claim 76, wherein said applying an ordered sequence of capture clocks further comprises applying a reversed ordered sequence of capture clocks from said ordered sequence of capture clocks for detecting or locating additional faults in said integrated circuit or circuit assembly.

87. (New) The method of claim 76, wherein said applying an ordered sequence of capture clocks further comprises selectively applying a shortened or expanded ordered sequence of capture clocks from said ordered sequence of capture clocks for detecting or locating additional faults in said integrated circuit or circuit assembly.

88. (New) The method of claim 76, wherein said applying an ordered sequence of capture clocks further comprises disabling one or more capture clocks to facilitate fault diagnosis.

89. (New) The method of claim 76, wherein said applying an ordered sequence of capture clocks further comprises selectively operating said capture clock at a selected clock speed for detecting or locating stuck-at faults within the clock domain controlled by said capture clock.

90. (New) The method of claim 76, wherein said applying an ordered sequence of capture clocks further comprises selectively operating said capture clock at its rated clock speed for detecting or locating delay faults within the clock domain controlled by said capture clock.

91. (New) The method of claim 76, wherein said applying an ordered sequence of capture clocks further comprises selectively reducing said capture clock speed to the level where delay faults associated with all multiple-cycle paths of equal cycle latency within the clock domain controlled by said capture clock are tested at a predetermined rated clock speed.

92. (New) The method of claim 76, wherein said applying an ordered sequence of capture clocks further comprises selectively operating two said capture clocks at selected clock speeds for detecting or locating stuck-at faults crossing two said clock domains.

93. (New) The method of claim 76, wherein said applying an ordered sequence of capture clocks further comprises selectively adjusting the relative clock delay of two said capture clocks operating at selected clock speeds for detecting or locating delay faults crossing two said clock domains.

94. (New) The method of claim 76, wherein said applying an ordered sequence of capture clocks further comprises selectively adjusting the relative clock delay of two said capture clocks to the level where delay faults associated with all multiple-cycle paths of equal cycle latency crossing two said clock domains are tested at a predetermined rated clock speed.

95. (New) The method of claim 76, wherein said applying an ordered sequence of capture clocks further comprises controlling the relative clock delay between any two adjacent capture clocks internally or external to said integrated circuit or circuit assembly.

96. (New) The method of claim 76, wherein said compacting N output responses further comprises using a plurality of multiple-input signature registers (MISRs) to generate said signatures.

97. (New) The method of claim 96, wherein said multiple-input signature register (MISR) further comprises using a space compactor connected to said MISR inputs for compressing said output responses to generate one or more said signatures.

98. (New) The method of claim 97, wherein said space compactor is a linear logic network comprising one or more Exclusive-OR (XOR) or Exclusive-NOR (XNOR) gates.

99. (New) The method of claim 76, further comprising using a PRPG-MISR (pseudorandom pattern generator and multiple-input signature register) pair to detect or locate said faults within a plurality of clock domains when the capture clocks controlling said plurality of clock domains operate at the same clock speed; wherein said capture clocks are selectively skewed so as to eliminate races and timing violation during said shift-in, said capture, or said compact operation.

100. (New) The method of claim 99, wherein said PRPG-MISR pair further comprises a PRPG, selectively a phase shifter, selectively a space compactor, a MISR, and selectively a comparator.

101. (New) The method of claim 100, wherein said PRPG-MISR pair further comprises connecting said PRPG and said MISR to the first-arrived capture clock and the last-arrived capture clock controlling said plurality of clock domains, respectively.

102. (New) The method of claim 76, wherein said compacting N output responses further comprises selectively comparing said N output responses directly with their expected output responses and indicating errors immediately using a compare operation.

103. (New) The method of claim 76, wherein said scan cell is selectively a multiplexed D flip-flop or a level-sensitive scan latch, and further wherein said integrated circuit or circuit assembly under test is a full-scan or partial-scan design.

104. (New) The method of claim 76, wherein said faults further comprise stuck-at faults and delay faults; wherein said stuck-at faults further comprise other stuck-type faults, such as open faults and bridging faults, and wherein said delay faults further comprise

other non-stuck-type delay faults, such as transition (gate-delay) faults, multiple-cycle delay faults, and path-delay faults.

105. (New) An apparatus for providing ordered capture clocks to detect or locate faults within N clock domains and faults crossing any two clock domains in an integrated circuit or circuit assembly in self-test mode, where N > 1, each clock domain having one capture clock and a plurality of scan cells, each capture clock comprising a plurality of shift clock pulses and capture clock pulses; said apparatus comprising:

(a) means for generating and shifting-in N pseudorandom stimuli to all said scan cells within said N clock domains in said integrated circuit or circuit assembly during a shift-in operation;

(b) means for applying an ordered sequence of capture clocks to all said scan cells within said N clock domains, the ordered sequence of capture clocks comprising at least two said capture clock pulses from two or more selected capture clocks placed in a sequential order, wherein each said selected capture clock must contain at least one said capture clock pulse and does not contain any said shift clock pulse, during a capture operation; and

(c) means for compacting N output responses of all said scan cells to signatures during a compact operation.

106. (New) The apparatus of claim 105, wherein said means of (a)-(c) are placed inside or external to said integrated circuit or circuit assembly.

107. (New) A method for providing ordered capture clocks to detect or locate faults within N clock domains and faults crossing any two clock domains in an integrated circuit or circuit assembly in self-test mode, where $N > 1$, each clock domain having one capture clock and a plurality of scan cells, each capture clock comprising a plurality of shift clock pulses and capture clock pulses; said method comprising the steps of:

(a) shifting-in N pseudorandom stimuli to all said scan cells within said N clock domains in said integrated circuit or circuit assembly during a shift-in operation;

(b) applying an ordered sequence of capture clocks to all said scan cells within said N clock domains, the ordered sequence of capture clocks comprising at

least two said capture clock pulses from two or more selected capture clocks placed in a sequential order, wherein each said selected capture clock must contain at least one said capture clock pulse and does not contain any said shift clock pulse, during a capture operation; and

(c) shifting-out N output responses of all said scan cells for analysis during a shift-out operation.

108.(New) The method of claim 107, further comprising providing N scan enable (SE) signals each within one said clock domain; wherein said SE signals are used to switch operations from shift-in/shift-out to capture, and vice versa; and further said SE signals can be generated internally or controlled externally, and are operated either at the rated clock speeds or at selected clock speeds.

109.(New) The method of claim 108, wherein said providing N scan enable (SE) signals further comprises using one global scan enable (GSE) signal to drive said N scan enable (SE) signals so that all said GSE and said SE signals can be operated at a selected reduced clock speed.

110. (New) A method for providing ordered capture clocks to detect or locate faults within N clock domains and faults crossing any two clock domains in an integrated

circuit or circuit assembly in scan-test mode, where N > 1, each clock domain having one capture clock and a plurality of scan cells, each capture clock comprising a plurality of shift clock pulses and capture clock pulses; said method comprising the steps of:

(a) generating and shifting-in N predetermined stimuli to all said scan cells within said N clock domains in said integrated circuit or circuit assembly during a shift-in operation;

(b) applying an ordered sequence of capture clocks to all said scan cells within said N clock domains, the ordered sequence of capture clocks comprising at least three said capture clock pulses from two or more selected capture clocks placed in a sequential order, wherein one said selected capture clock must contain at least two said capture clock pulses and does not contain any said shift clock pulse, during a capture operation; and

(c) comparing N output responses directly with their expected output responses for all said scan cells within said N clock domains and indicating errors immediately during a compare operation.

111. (New) The method of claim 110, wherein each said capture clock is programmable to contain one or more clock pulses for performing said shift-in/compare and capture

operations on all said scan cells within one said clock domain; wherein said clock domain is solely controlled by said capture clock; and said capture clock can be either generated internally or controlled externally, and can operate either at its rated clock speed (at-speed) or at a selected clock speed.

112. (New) The method of claim 110, further comprising providing N scan enable (SE) signals each within one said clock domain; wherein said SE signals are used to switch operations from shift-in/compare to capture, and vice versa; and further said SE signals can be generated internally or controlled externally, and are operated either at the rated clock speeds or at selected clock speeds.

113. (New) The method of claim 112, wherein said providing N scan enable (SE) signals further comprises using one global scan enable (GSE) signal to drive said N scan enable (SE) signals so that all said GSE and said SE signals can be operated at a selected reduced clock speed.

114. (New) The method of claim 110, wherein said generating and loading N predetermined stimuli further comprises operating all said N capture clocks at selected clock speeds or at the same clock speed; wherein all said N capture clocks

are selectively skewed so that at any given time only scan cells within one or more said clock domains are changing states to reduce power consumption.

115.(New) The method of claim 110, wherein said applying an ordered sequence of capture clocks further comprises applying two or more said capture clocks concurrently on clock domains which do not interact with each other or have any logic block crossing each other for detecting or locating said faults in said clock domains controlled by said capture clocks.

116. (New) The method of claim 110, wherein said applying an ordered sequence of capture clocks further comprises applying a reversed ordered sequence of capture clocks from said ordered sequence of capture clocks for detecting or locating additional faults in said integrated circuit or circuit assembly.

117. (New) The method of claim 110, wherein said applying an ordered sequence of capture clocks further comprises selectively applying a shortened or expanded ordered sequence of capture clocks from said ordered sequence of capture clocks for detecting or locating additional faults in said integrated circuit or circuit assembly.

118. (New) The method of claim 110, wherein said applying an ordered sequence of capture clocks further comprises disabling one or more capture clocks to facilitate fault diagnosis.

119.(New) The method of claim 110, wherein said applying an ordered sequence of capture clocks further comprises selectively operating said capture clock at a selected clock speed for detecting or locating stuck-at faults within the clock domain controlled by said capture clock.

120. (New) The method of claim 110, wherein said applying an ordered sequence of capture clocks further comprises selectively operating said capture clock at its rated clock speed for detecting or locating delay faults within the clock domain controlled by said capture clock.

121. (New) The method of claim 110, wherein said applying an ordered sequence of capture clocks further comprises selectively reducing said capture clock speed to the level where delay faults associated with all multiple-cycle paths of equal cycle latency within the clock domain controlled by said capture clock are tested at a predetermined rated clock speed.

122.(New) The method of claim 110, wherein said applying an ordered sequence of capture clocks further comprises selectively operating two said capture clocks at selected clock speeds for detecting or locating stuck-at faults crossing two said clock domains.

123.(New) The method of claim 110, wherein said applying an ordered sequence of capture clocks further comprises selectively adjusting the relative clock delay of two said capture clocks operating at selected clock speeds for detecting or locating delay faults crossing two said clock domains.

124. (New) The method of claim 110, wherein said applying an ordered sequence of capture clocks further comprises selectively adjusting the relative clock delay of two said capture clocks to the level where delay faults associated with all multiple-cycle paths of equal cycle latency crossing two said clock domains are tested at a predetermined rated clock speed.

125. (New) The method of claim 110, wherein said applying an ordered sequence of capture clocks further comprises controlling the relative clock delay between any two adjacent capture clocks internally or external to said integrated circuit or circuit assembly.

126.(New) The method of claim 110, wherein said comparing N output responses directly with their expected output responses further comprises selectively compacting said N output responses to signatures using a compact operation.

127. (New) The method of claim 126, wherein said compacting N output responses to signatures further comprises comparing said signatures with their expected signatures after a predetermined limiting criterion is reached; wherein said comparing said signatures with their expected signatures further comprises comparing said signatures inside said integrated circuit or circuit assemble, or shifting-out said signatures for comparison in an ATE (automatic test equipment).

128. (New) The method of claim 110, wherein said scan cell is selectively a multiplexed D flip-flop or a level-sensitive scan latch, and further wherein said integrated circuit or circuit assembly under test is a full-scan or partial-scan design.

129. (New) The method of claim 110, wherein said faults further comprise stuck-at faults and delay faults; wherein said stuck-at faults further comprise other stuck-type faults, such as open faults and bridging faults, and wherein said delay faults further comprises other non-stuck-type delay faults, such as transition (gate-delay) faults, multiple-cycle delay faults, and path-delay faults.

130.(New) An apparatus for providing ordered capture clocks to detect or locate faults within N clock domains and faults crossing any two clock domains in an integrated circuit or circuit assembly in scan-test mode, where N > 1, each clock domain having one capture clock and a plurality of scan cells, each capture clock comprising a plurality of shift clock pulses and capture clock pulses; said apparatus comprising:

(a) means for generating and shifting-in N predetermined stimuli to all said scan cells within said N clock domains in said integrated circuit or circuit assembly during a shift-in operation;

(b) means for applying an ordered sequence of capture clocks to all said scan cells within said N clock domains, the ordered sequence of capture clocks comprising at least three said capture clock pulses from two or more selected capture clocks placed in a sequential order, wherein one said selected capture clock must contain at least two said capture clock pulses and does not contain any said shift clock pulse, during a capture operation; and

(c) means for comparing N output responses directly with their expected output responses for all said scan cells within said N clock domains and indicating errors immediately during a compare operation.

131.(New) The apparatus of claim 130, wherein said means of (a)-(c) are placed inside or external to said integrated circuit or circuit assembly.

132. (New) A method for providing ordered capture clocks to detect or locate faults within N clock domains and faults crossing any two clock domains in an integrated circuit or circuit assembly in scan-test mode, where N > 1, each clock domain having one capture clock and a plurality of scan cells, each capture clock comprising a plurality of shift clock pulses and capture clock pulses; said method comprising the steps of:

(a) shifting-in N predetermined stimuli to all said scan cells within said N clock domains in said integrated circuit or circuit assembly during a shift-in operation;

(b)applying an ordered sequence of capture clocks to all said scan cells within said N clock domains, the ordered sequence of capture clocks comprising at least three said capture clock pulses from two or more selected capture clocks placed in a sequential order, wherein one said selected capture clock must contain at least two said capture clock pulses and does not contain any said shift clock pulse, during a capture operation; and

(c) shifting-out N output responses of all said scan cells for analysis during a shift-out operation.

133. (New) The method of claim 132, further comprising providing N scan enable (SE) signals each within one said clock domain; wherein said SE signals are used to switch operations from shift-in/shift-out to capture, and vice versa; and further said SE signals can be generated internally or controlled externally, and are operated either at the rated clock speeds or at selected clock speeds.

134. (New) The method of claim 133, wherein said providing N scan enable (SE) signals further comprises using one global scan enable (GSE) signal to drive said N scan enable (SE) signals so that all said GSE and said SE signals can be operated at a selected reduced clock speed.